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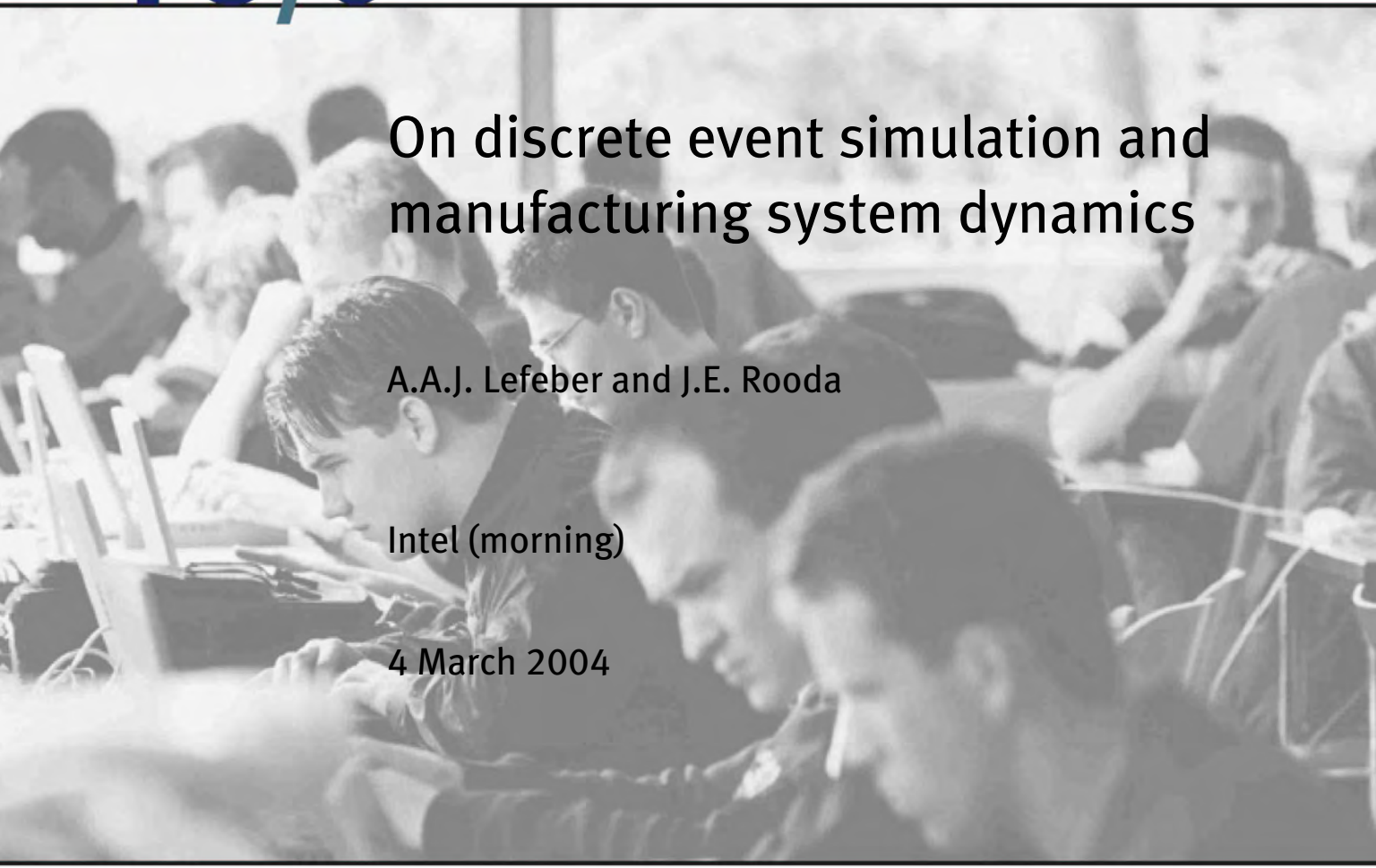

On discrete event simulation and manufacturing system dynamics

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Intel (morning)

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/department of mechanical engineering

Outline

- discrete event simulation
  - a detailed model
  - effective process times
- understanding dynamics
  - a ramp up study
  - a second ramp up study

Production characteristics

- 161 equipments
- over 300 process steps
- 20 layers per wafer
- several wafer types (routings)
- normal lots and priority lots
- large unscheduled down times
- re-entrant flow shop

Model

- discrete-event simulation
- processes; generator, buffer and equipments
- communications: lots and information
- equipments

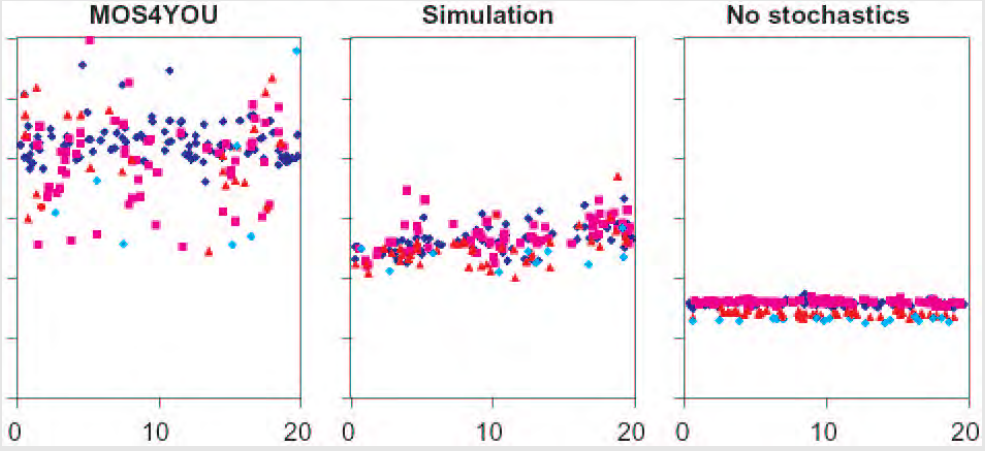
  EB batch (Furnace)

  EC cascade (Litho, Wetbench)

  EI ion

  EM measure

Results



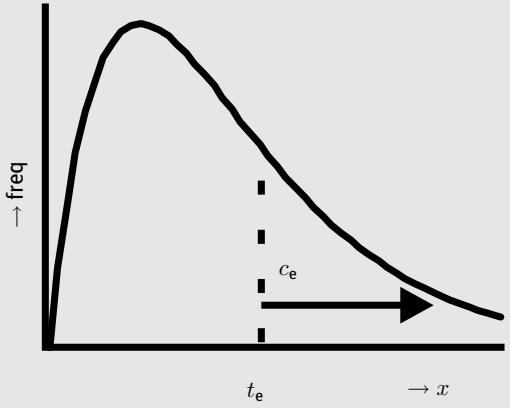
- smaller mean flow time
- smaller variance flow time

The effective process time method

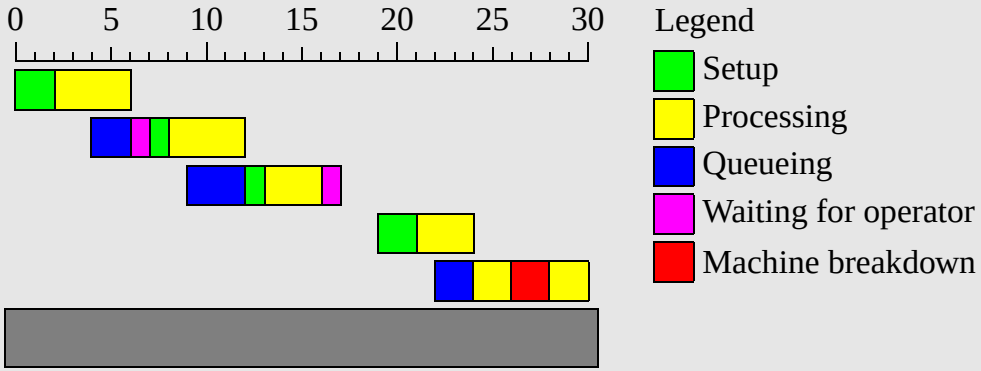
- raw process time t_0 and c_0
- setups t_s and c_s
- TBF t_f and c_f, TTR t_r and c_r
- operator delays
- rework
- . . . (!)

Idea:

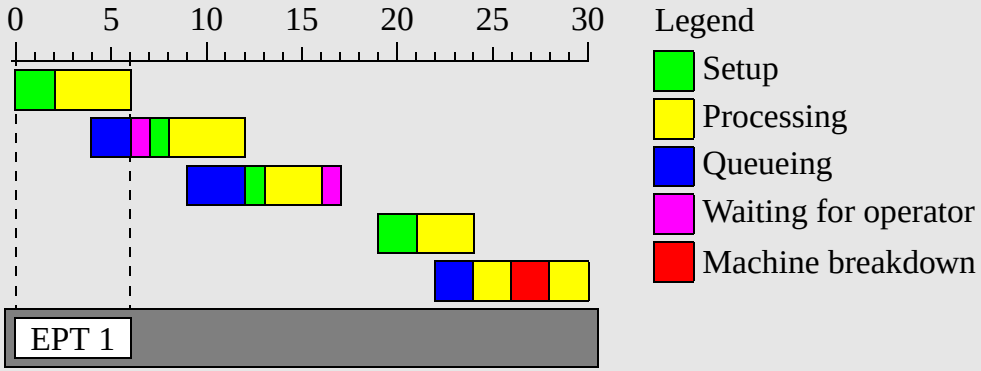
Combine all disturbances in one single EPT probability density function



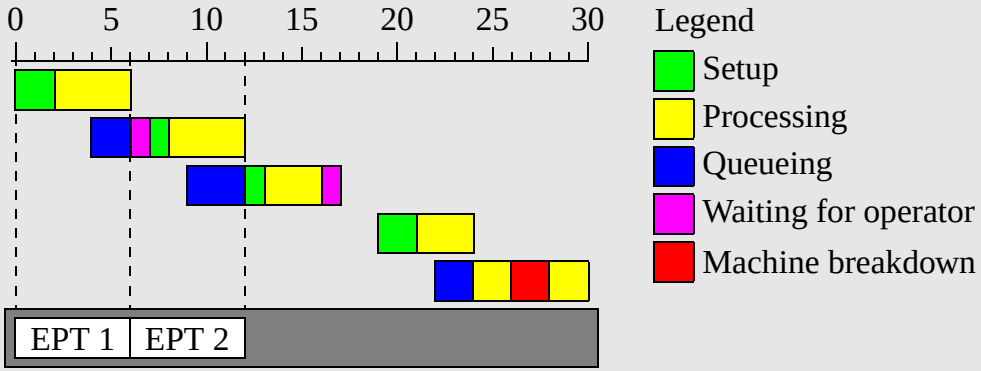
Effective process times



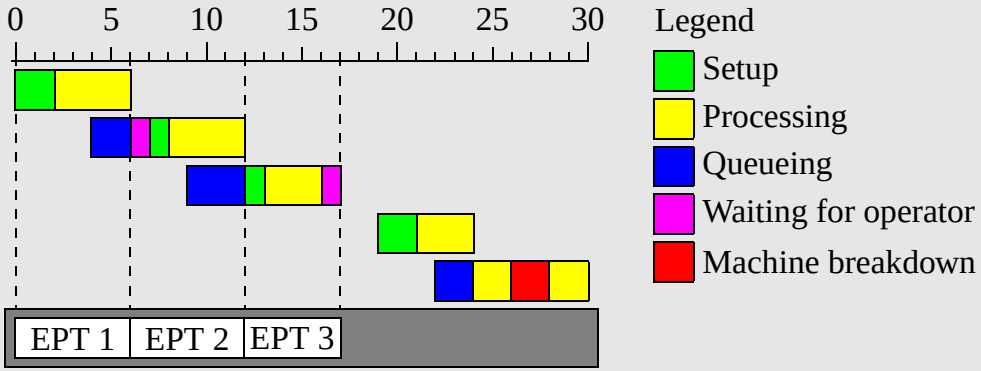
Effective process times



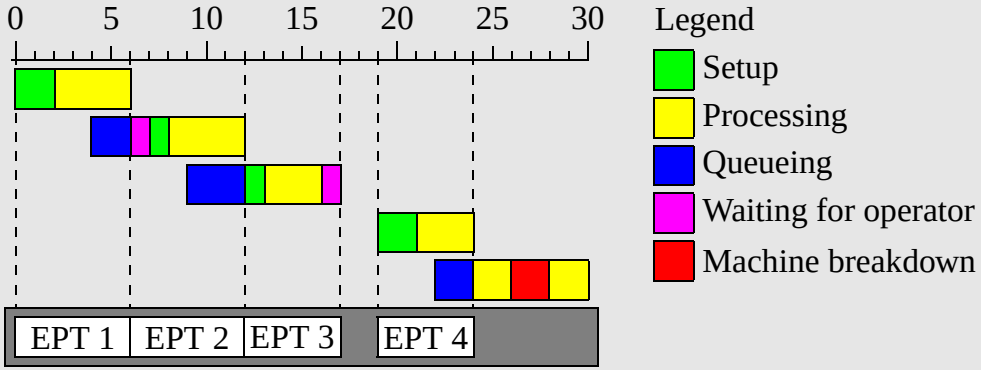
Effective process times



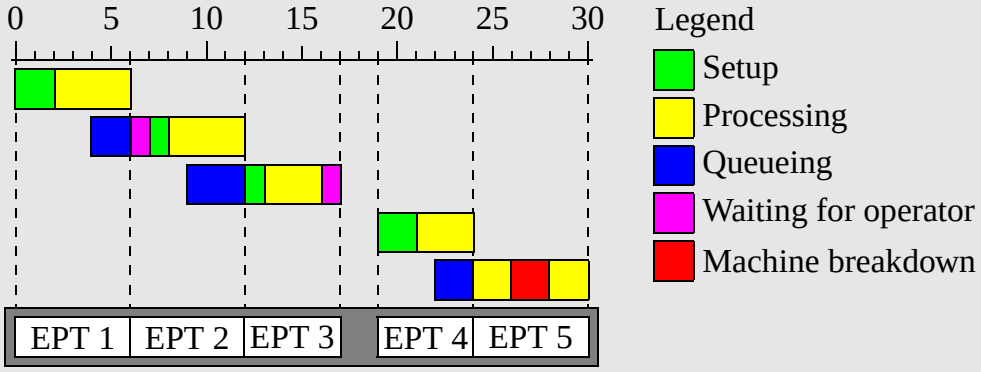
Effective process times



Effective process times



Effective process times



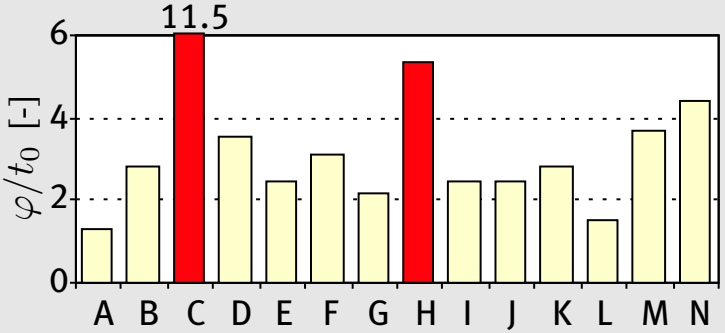
Semiconductor wafer fab case

Measured data:
Track-in and track-out data
Fourteen equipment families with only single-lot machines
Data from 6 months

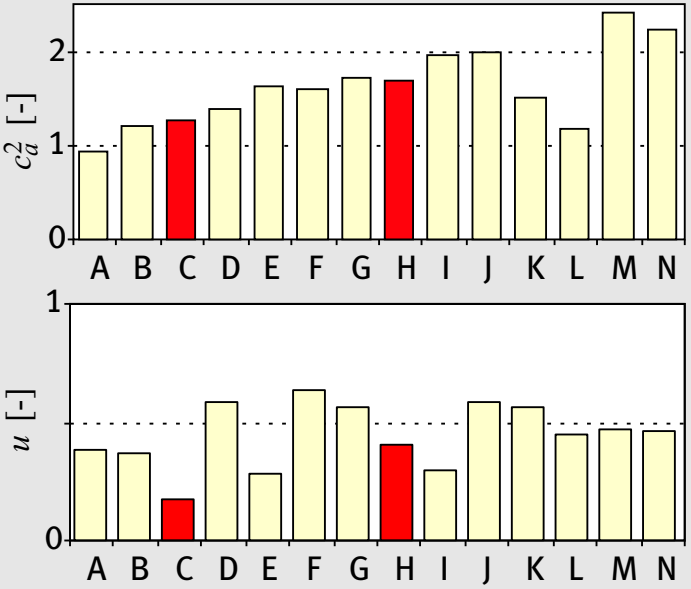
Results:

φ	mean flow time in workstation
t_0	mean raw process time
c_0^2	squared coefficient of variation of t_0
u	utilization
c_{a}^2	squared coefficient of variation of inter arrival time t_{a}
t_{e}	mean effective process time
c_{e}^2	squared coefficient of variation of t_{e}

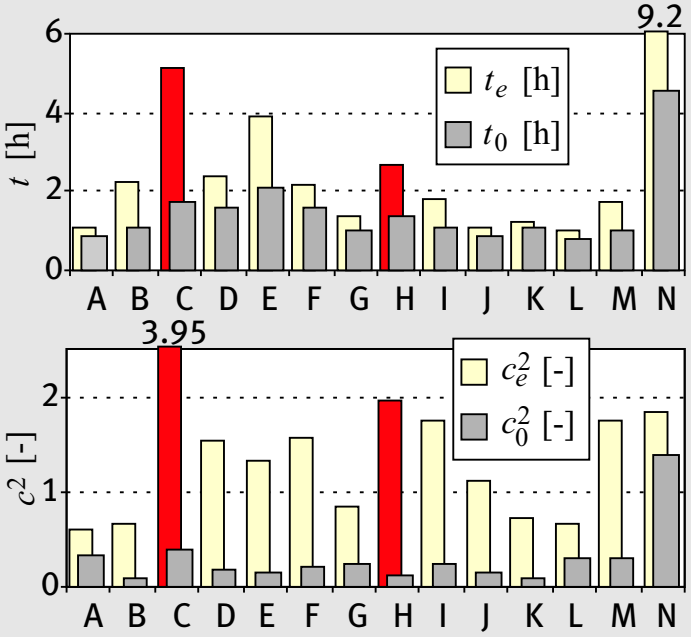
Semiconductor wafer fab case



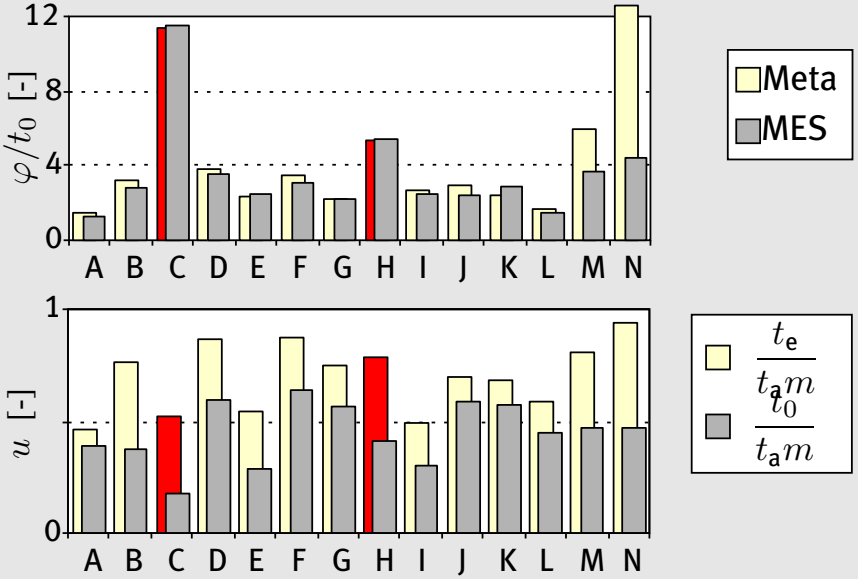
Semiconductor wafer fab case



Semiconductor wafer fab case



Semiconductor wafer fab case



Outline

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Case

L.M. Wein. Scheduling semiconductor wafer fabrication. IEEE TSM, 1(3):115–129, 1988

No.	Name	Operation	Fab 1	Fab 2	Fab 3	NV/L	MPT
1	CLEAN	Deposition	2	2	1	19	1.55
2	TMGOX	Deposition	2	2	1	5	4.98
3	TMNOX	Deposition	2	2	1	5	5.45
4	TMFOX	Deposition	1	1	1	3	4.68
5	TU11	Deposition	1	1	1	1	6.14
6	TU43	Deposition	1	1	1	2	7.76
7	TU72	Deposition	1	1	1	1	6.23
8	TU73	Deposition	1	1	1	3	4.35
9	TU94	Deposition	1	1	1	2	4.71
10	PLM5L	Deposition	1	1	1	3	4.05
11	PLM5U	Deposition	1	1	1	1	7.86
12	SPUT	Lithography	1	1	2	2	6.1
13	PHPPS	Lithography	4	4	3	13	4.23
14	PHGCA	Lithography	3	3	1	12	7.82
15	PHHB	Lithography	1	1	1	15	0.87
16	PHBI	Lithography	2	2	1	11	2.96
17	PHFI	Lithography	1	1	1	10	1.56
18	PHJPS	Lithography	1	1	1	4	3.59
19	PLM6	Etching	2	2	1	2	13.88
20	PLM7	Etching	1	1	1	2	5.41
21	PLM8	Etching	2	2	1	4	7.58
22	PHWET	Etching	2	2	1	21	1.04
23	PHPLO	Resist strip	2	2	1	23	1.09
24	IMP	Ion implant	2	1	1	8	3.86

Case

- Recipe: 172 steps
- Processing times: exponential
- Batch size: 1 (no batching)
- Cascade machine (litho): after 80% of processing time has passed new lot can be started

- Formalism chi (χ-0.7)
- General recipe (read from file)
- General fab-layout (read from file)

Ramp up policies

Policy A:
- Release all WIP at once
- Use CONWIP

Policy B:
- Release lots at desired output rate

Policy D:
- Use higher rate, until 1^{st} lot leaves fab
- From then on: feed at desired output rate

Policy E:
- Use higher rate, until desired WIP level
- From then on: apply CONWIP

Scheduling policies

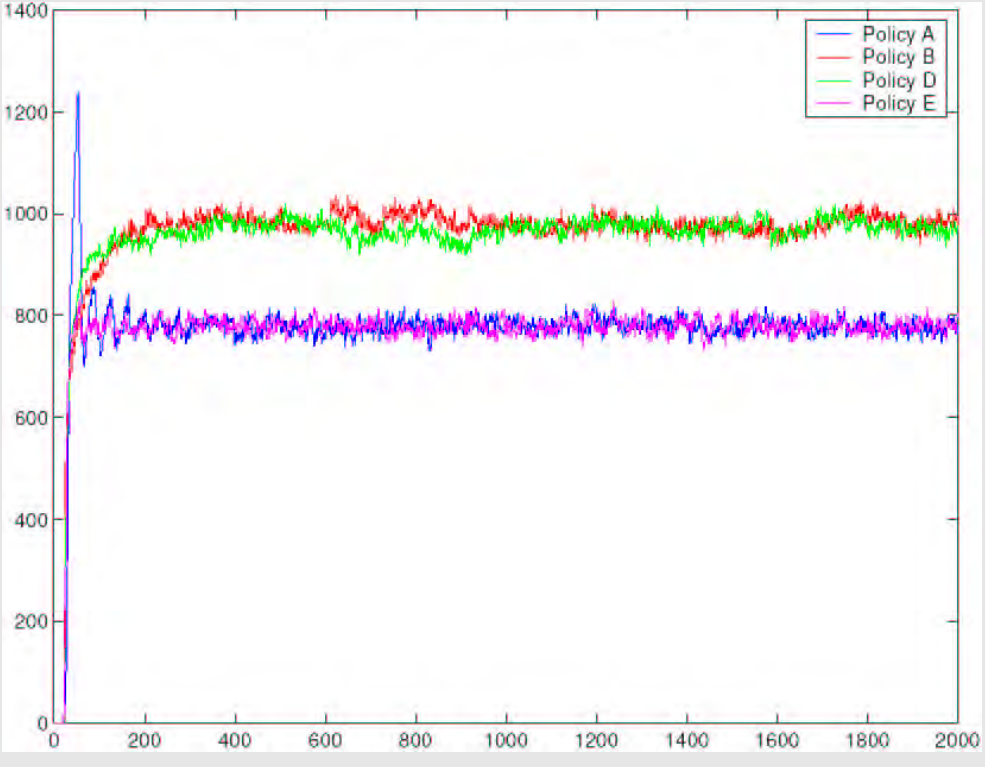
- FIFO
- Push/FBFS: priority to 'younger' lots
- Pull/LBFS: priority to 'older' lots

Experiment

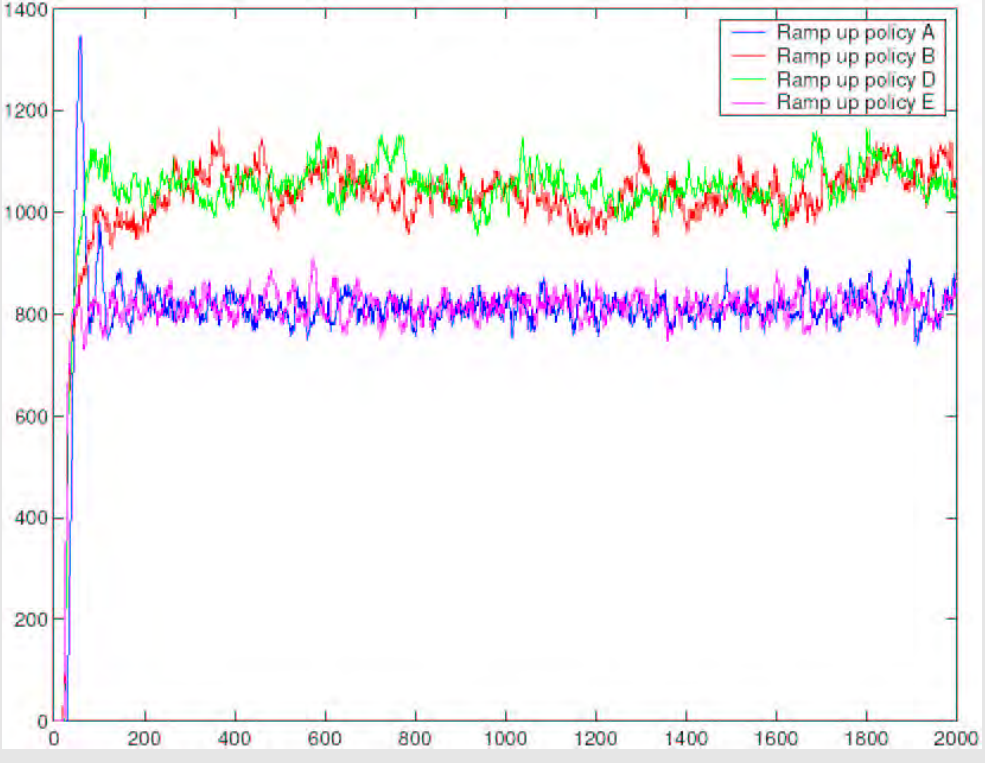
- Utilization 95%
- Higher rate: utilization 113.6%
- Run length: 2000 days
- CONWIP-level: mean WIP at u=95% (using FIFO)
- At least 30 experiments

  Extra, until 95%-confidence interval of *mean flow time after 2000 days* has width ≤ 0.05

FIFO


Policy A
Policy B
Policy D
Policy E
1400
1200
1000
800
600
400
200
0
0
200
400
600
800
1000
1200
1400
1600
1800
2000

Push/FBFS


Ramp up policy A
Ramp up policy B
Ramp up policy D
Ramp up policy E
1400
1200
1000
800
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400
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0
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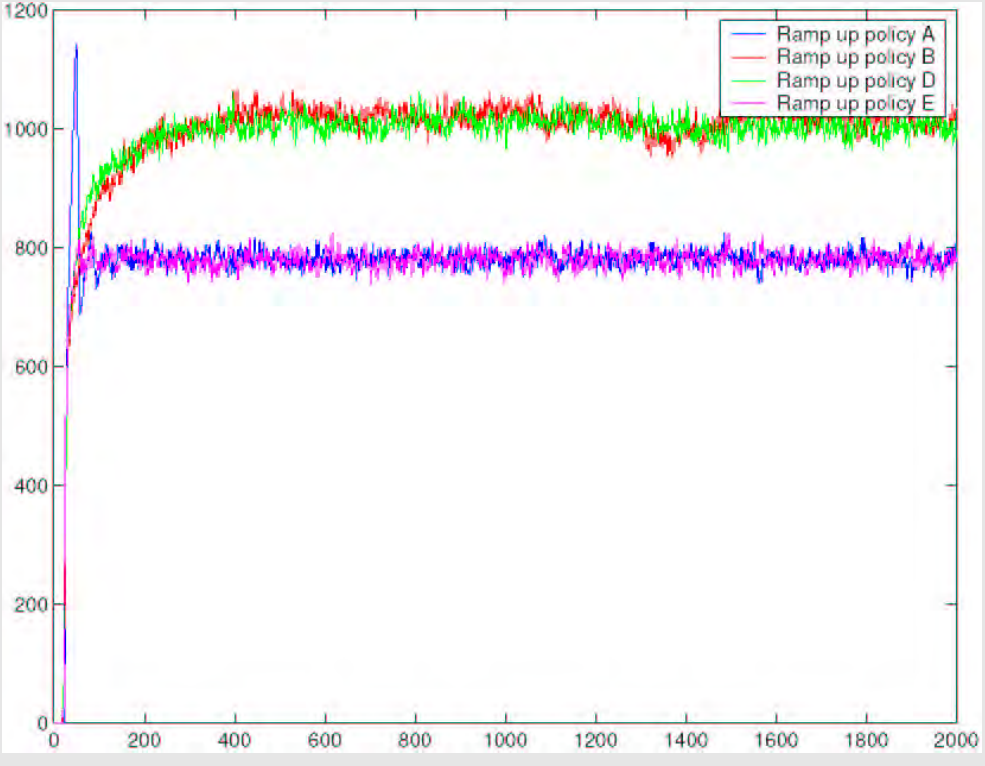
200
400
600
800
1000
1200
1400
1600
1800
2000

Pull/LBLS


Ramp up policy A
Ramp up policy B
Ramp up policy D
Ramp up policy E
1200
1000
800
600
400
200
0
0
200
400
600
800
1000
1200
1400
1600
1800
2000

Conclusions

- Policy A and E better than B and D: same WIP-level, lower flow time (constant WIP better than push)
- Behavior of ramp up policy similar for each scheduling rule
- Scheduling by Push/FBFS (slightly) higher flow times
- Similar results for FIFO and Pull/LBFS
- Influence of scheduling relatively low

A second ramp up study

Case

- Line of 15 identical workstations
- Infinite buffers (FIFO)
- Processing times: exponential (mean 1.0)
- Inter arrival times: exponential (mean $1/\lambda$)

Experiments

- From one steady state to the other
- ramp up: from initially empty to 25%, 50%, 75%, 90%, 95% utilization
- Batches of 1000 experiments
- 1000 batches (99% confidence interval: relative width less than 0.01 for utilization of 95%)

- MOVIE

Conclusions

First part

- Introduced effective processing times for obtaining simpler meta-models

Ramp up study I:

- CONWIP better than push
- Start policy more relevant than buffering policy

Ramp up study II:

- Movies, generated from several discrete event simulations, provide insight in dynamics

Overall conclusion

- Discrete event simulation can provide insight in *dynamics*, not only steady state